CLAIMS:

1. A filter arrangement for filtering digital data comprising synchronizing information, in which the arrangement operates in a system clock, characterized in that the arrangement comprises a first filter (1) and a second, succeeding filter (2) which supplies the output signal of the arrangement, in that the first filter (1) receives at least the synchronizing information comprised in the data and the second filter (2) receives the output signal of the first filter (1) as well as the digital data, in that the first filter (1) searches synchronizing information in a cyclically repeating process, passes on this information to its output, subsequently blocks all possibly occurring synchronizing information during a predetermined number of system clock pulses, and, after finishing the predetermined number of system clocks, again searches and passes on the next synchronizing information, and in that the second filter (2) takes over a predetermined number of data from the data signal in a cyclically repeating process from synchronizing information supplied by the first filter (1), and passes on these data to its output and blocks subsequent data until the next synchronizing information supplied by the first filter (1), from which synchronizing information the predetermined number of data is taken over again from the data signal and passed on to the output.

2. An arrangement as claimed in claim 1, characterized in that the arrangement comprises a separating stage (4) which separates the synchronizing information applied to the first filter (1) from the digital data.

3. An arrangement as claimed in claim 1, characterized in that the data of an acquisition stage (3) provided in the arrangement are supplied in a first external clock which is not coupled to the system clock, and in that the acquisition stage (3) determines with which pulses of the system clock a valid new data bit of the serial data is present, and which applies a corresponding acquisition signal to the second filter (2).

4. An arrangement as claimed in claims 1 and 3, characterized in that the predetermined number of system clock pulses is implemented in such a way that processes

succeeding the filter arrangement can still process the data rate of the output signal of the arrangement, and in that the predetermined number of data is implemented in such a way that all data between two synchronizing information components are taken over when the external clock has a nominal clock frequency.

5. An arrangement as claimed in claim 1, characterized in that the data are video data which are present in the form of data words.

6. An arrangement as claimed in claim 5, characterized in that the first filter (1) evaluates vertical synchronizing pulses comprised as synchronizing information in the video data.

7. An arrangement as claimed in claim 5, characterized in that the second filter (2) evaluates the vertical synchronizing pulses supplied by the first filter as synchronizing information and additionally orders the data in dependence upon horizontal synchronizing pulses.

8. An arrangement as claimed in claim 1, characterized in that the arrangement precedes a memory (5) in which the output data of the second filter (2) are stored in an ordered manner in dependence upon the synchronizing information.

9. An arrangement as claimed in claim 8, characterized in that the arrangement precedes an MPEG encoding process (6) which accesses the data stored in the memory (5), and in that the second filter (2) supplies a filling level signal indicating the filling level of the data in the memory (5) for the MPEG encoding process (6).